IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

In re Application of:	:	
	:	Group Art Unit: 2825
Herman Kwong et al.	:	
	:	Examiner: Yelena Rossoshek
Appln. No.: 10/728,894	:	
	:	Confirmation No.: 9607
Filed: December 8, 2003	:	
	:	Customer No.: 21967
For: CONTACT MAPPING USING CHANNEL ROUTING	:	

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Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

APPEAL BRIEF

Sir:

In response to the Office Action dated November 3, 2006, finally rejecting pending claims 1-18, Appellants respectfully request that the Board of Patent Appeals and Interferences reconsider and withdraw the rejections of record, and allow the pending claims, which are attached hereto.

REAL PARTY IN INTEREST

The Appellants, Herman Kwong et al., are the Applicants in the above-identified patent application. The Appellants have assigned their entire interest in the above-identified patent application to Nortel Networks Limited, 2351 Boulevard Alfred-Nobel, St. Laurent, Quebec, H4S 2A9 Canada.

RELATED APPEALS AND INTERFERENCES

The Appellants, the Appellants' legal representative, and the Assignee are not aware of any other appeals or interferences which will directly affect, be directly affected by, or have a bearing on the Board's decision in this Appeal.

STATUS OF CLAIMS

Claims 1-18 are pending in the above-identified patent application. Claims 1-18 were finally rejected in the Office Action dated November 3, 2006 (hereinafter "Office Action"). The final rejection of claims 1-18 is hereby appealed.

Claims 1-18 stand rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 5,877,942 to Kida *et al.* (hereinafter "Kida").

STATUS OF AMENDMENTS

Amendments to claims 1, 10, and 15 were filed subsequent to the final rejection of claims 1-18 in the Office Action dated November 3, 2006. However, these amendments were not entered by the Examiner.

SUMMARY OF CLAIMED SUBJECT MATTER

The claimed invention, as set forth in claim 1, and as described and shown in the Specification and Figures 1-7 of the above-identified patent application, respectively, is directed to a method for mapping contacts of a programmable logic device (PLD) to contacts of an electronic component in a signal routing device having one or more layers. *See*, e.g., page 4, lines 14-17. The method comprises assigning a set of one or more contacts (e.g., 220-254) of the PLD (e.g., 106) to one or more respective contacts (e.g., 120-154) of the electronic component (e.g., 104) based at least in part on a pattern of electrically conductive traces (e.g., 160-194) routed from respective contacts of the electronic component via one or more channels (e.g., 110, 112, 114) formed at one or more layers of the signal routing device (e.g., 108), the one or more channels being formed by arranging vias (e.g., 202-216) for contacts of at least the electronic component in the signal routing device.

See, e.g., Figures 1 and 2; page 4, lines 17-23; page 10, lines 31-33; page 11, lines 1-7.

The claimed invention, as set forth in claim 10, and as described and shown in the Specification and Figures 1-7 of the above-identified patent application, respectively, is directed to a method for mapping contacts of a programmable logic device (PLD) to contacts of an electronic component in a signal routing device having one or more layers. *See*, e.g., page 4, lines 24-27. The method comprises determining (e.g., 702) a first pattern of electrically conductive traces routed from respective contacts of the electronic component via one or more channels formed at one or more layers of the signal routing device. *See*, e.g., Figure 7; page 4, lines 27-31; page 17, lines 29-33; page 18, lines 1-2. The method also comprises determining (e.g., 704) a first contact assignment pattern for one or more contacts of the PLD based at least in part on the first pattern of electrically conductive traces. *See*, e.g., Figure 7; page 4, lines 31-32; page 5, lines 1-2; page 18, lines 3-5. The method further comprises refining (e.g., 706-708) the first pattern of electrically conductive traces based at least in part on the first contact assignment pattern to generate a second pattern of electrically conductive traces routed from the respective contacts of the electronic component via one or more channels

formed at one or more layers of the signal routing device. *See*, e.g., Figure 7; page 5, lines 2-7; page 18, lines 5-27. The method additionally comprises determining (e.g., 704-708) a second contact assignment pattern for one or more contacts of the PLD based at least in part on the second pattern of electrically conductive traces, wherein the one or more channels are formed by arranging vias for contacts of at least the electronic component in the signal routing device. *See*, e.g., Figure 7; page 5, lines 8-10; page 18, lines 28-33; page 19, lines 1-2.

The claimed invention, as set forth in claim 15, and as described and shown in the Specification and Figures 1-7 of the above-identified patent application, respectively, is directed to a signal routing device (e.g., 108) having one or more layers. *See*, e.g., page 5, lines 11-12. The signal routing device (e.g., 108) comprises an electronic component (e.g., 104) having a plurality of contacts (e.g., 120-154). *See*, e.g., Figures 1 and 2; page 5, lines 13-14; page 9, lines 27-30. The signal routing device (e.g., 108) also comprises a programmable logic device (PLD) (e.g., 106) having a plurality of contacts (e.g., 220-254). *See*, e.g., Figures 1 and 2; page 5, lines 14-15; page 11, lines 24-33. The signal routing device (e.g., 108) further comprises a plurality of electrically conductive traces

(e.g., 160-194) connecting contacts (e.g., 220-254) of the PLD (e.g., 106) to respective contacts (e.g., 120-154) of the electronic component (e.g., 104), the plurality of electrically conductive traces (e.g., 160-194) routed from the respective contacts (e.g., 120-154) of the electronic component (e.g., 104) via one or more channels (e.g., 110, 112, 114) formed at one or more layers of the signal routing device (e.g., 108), wherein the one or more contacts (e.g., 220-254) of the PLD (e.g., 106) are assigned based at least in part on a pattern formed by the electrically conductive traces (e.g., 160-194) routed from the respective contacts (e.g., 120-154) of the electronic component (e.g., 104) via the one or more channels (e.g., 110, 112, 114), wherein the one or more channels (e.g., 110, 112, 114) are formed by arranging vias (e.g., 202-216) for contacts of at least the electronic component (e.g., 104) in the signal routing device (e.g., 108). *See*, e.g., Figures 1 and 2; page 5, lines 15-25; page 9, lines 30-33; page 10, lines 1-33; page 11, lines 1-7.

GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

Claims 1-18 stand rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 5,877,942 to Kida *et al.* ("Kida").

ARGUMENT

The Appellants respectfully appeal the decision of the Examiner to finally reject claims 1-18 of the above-identified patent application.

I. THE ANTICIPATION REJECTION OF CLAIMS 1-18

The Examiner asserts that claims 1-18 should be rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 5,877,942 to Kida *et al.* ("Kida"). This rejection is respectfully traversed.

Under 35 U.S.C. § 102, the Patent Office bears the burden of presenting at least a prima facie case of anticipation. In re King, 801 F.2d 1324, 1326 (Fed. Cir. 1986). Anticipation requires that a prior art reference disclose, either expressly or under the principles of inherency, each and every element of the claimed invention. Celeritas Tech., Ltd., v. Rockwell Int'l Corp., 150 F.3d 1354, 1361 (Fed. Cir. 1998). The prior art reference must disclose all of the claim elements arranged or combined in the same way as recited in the claim. Net MoneyIN, Inc. v. VeriSign, Inc. (CAFC Appeal No. 2007-1565) (Fed. Cir. 2008). "In addition, the prior art reference must be enabling." Akzo N.V. v. U.S. International Trade Commission, 808 F.2d 1471,

1479 (Fed. Cir. 1986), cert. denied, 482 U.S. 909 (1987). That is, the prior art reference must sufficiently describe the claimed invention so as to have placed the public in possession of it. In re Donohue, 766 F.2d 531, 533 (Fed. Cir. 1985). Such possession is effected only if one of ordinary skill in the art could have combined the disclosure in the prior art reference with his/her own knowledge to make the claimed invention. Id..

A. THE EXAMINER HAS FAILED TO ESTABLISH A PRIMA FACIE CASE OF ANTICIPATION AGAINST CLAIM 1

Regarding claim 1, the Examiner asserts on pages 3-4 of the Office Action that Kida teaches the claimed invention. More specifically, the Examiner asserts that Kida teaches "assigning a set of one or more contacts of the PLD to one or more respective contacts of the electronic component based at least in part on a pattern of electrically conductive traces routed from respective contacts of the electronic component via one or more channels formed at one or more layers of the signal routing device, the one or more channels being formed by arranging vias for contacts of at least the electronic component in the signal routing device," as claimed. However, Appellants respectfully submit that the Examiner has erroneously interpreted the teachings of Kida. That is, Kida teaches:

> "providing pairs of near and far vias with the near and far vias of each pair interconnected on a surface of the apparatus by a severable trace and with all interconnection paths to or from terminal areas for use with user programmable input/output pins of the FPGA routed through at least one pair of near and far vias along at least one severable surface trace, such that selected interconnection paths of the apparatus are subject to re-working by severing selected ones of the severable traces on the surface of the apparatus and by adding jump wires over the surface of the apparatus between selected vias."

See, Column 4, lines 54-64 (emphasis added). Nowhere does Kida disclose, or even suggest, routing a pattern of electrically conductive traces "from respective contacts of the electronic component via one or more channels formed at one or more layers of the signal routing device, the one or more channels being formed by arranging vias for contacts of at least the electronic component in the signal routing device," as claimed. Indeed, Kida fails to disclose, or even suggest, in any manner, routing traces in channels and/or forming channels in one or more layers of a signal routing device by arranging vias for contacts of an electronic component in the signal routing device, as claimed. Further, Kida certainly fails to disclose, or even suggest, all of the claim elements arranged or combined in the same way as recited in the claim, as is required to establish a prima facie case of anticipation. Thus, Kida fails to disclose, or even suggest, "assigning a set of one or more contacts of the PLD to

one or more respective contacts of the electronic component based at least in part on a pattern of electrically conductive traces routed from respective contacts of the electronic component via one or more channels formed at one or more layers of the signal routing device, the one or more channels being formed by arranging vias for contacts of at least the electronic component in the signal routing device," as claimed.

In view of the foregoing, is it respectfully submitted that claim 1 is allowable over Kida.

B. THE EXAMINER HAS FAILED TO ESTABLISH A PRIMA FACIE CASE OF ANTICIPATION AGAINST CLAIMS 2-9

Regarding claims 2-9, these claims are dependent upon independent claim 1. Thus, since independent claim 1 should be allowable as discussed above, claims 2-9 should also be allowable at least by virtue of their dependency on independent claim 1. Moreover, these claims recite additional features which are not disclosed, or even suggested, by Kida. Thus, these claims are separately patentable over Kida for at least the reasons stated below.

Appellants note that the Examiner asserts in the Office Action that claims 2-9 are rejected based upon Taylor. *See*, e.g., Office Action, page 6. The Examiner has failed to explicitly assert an obviousness rejection based upon the

combination of Kida and Taylor in the Office Action. The Examiner has also failed to explicitly assert an anticipation rejection based upon Taylor alone in the Office Action. Thus, Appellants respectfully request correction of the record in this regard.

1. THE EXAMINER HAS FAILED TO ESTABLISH A PRIMA FACIE CASE OF ANTICIPATION AGAINST CLAIM 2

Claim 2 is separately patentable because Kida fails to disclose forming electrically conductive traces between the set of one or more contacts of the PLD and the respective contacts of the electronic component in accordance with the pattern of electrically conductive traces, as claimed. The rejection of this claim is thus improper for the reasons set forth above with respect to claim 1. In addition, Kida fails to show each and every limitation of claim 2.

2. THE EXAMINER HAS FAILED TO ESTABLISH A PRIMA FACIE CASE OF ANTICIPATION AGAINST CLAIM 3

Claim 3 is separately patentable because Kida fails to disclose that one or more of the electrically conductive traces are routed to respective contacts of the PLD via one or more channels formed at one or more layers of the signal routing device, as claimed. The rejection of this claim is thus

improper for the reasons set forth above with respect to claim 1. In addition, Kida fails to show each and every limitation of claim 3.

3. THE EXAMINER HAS FAILED TO ESTABLISH A PRIMA FACIE CASE OF ANTICIPATION AGAINST CLAIM 4

Claim 4 is separately patentable because Kida fails to disclose determining a first pattern of electrically conductive traces routed from respective contacts of the electronic component via at least one channel of the one or more channels, determining a contact assignment pattern for one or more contacts of the PLD based at least in part on the first pattern of electrically conductive traces, and refining the first pattern of electrically conductive traces based at least in part on the first contact assignment pattern to generate a second pattern of electrically conductive traces routed from the respective contacts of the electronic component via at least one of the one or more channels, as claimed. The rejection of this claim is thus improper for the reasons set forth above with respect to claim 1. In addition, Kida fails to show each and every limitation of claim 4.

4. THE EXAMINER HAS FAILED TO ESTABLISH A PRIMA FACIE CASE OF ANTICIPATION AGAINST CLAIM 5

Claim 5 is separately patentable because Kida fails to disclose that the one or more contacts of the PLD are assigned to the one or more respective contacts of the electronic component based at least in part on the second pattern of electrically conductive traces, as claimed. The rejection of this claim is thus improper for the reasons set forth above with respect to claim 1. In addition, Kida fails to show each and every limitation of claim 5.

5. THE EXAMINER HAS FAILED TO ESTABLISH A PRIMA FACIE CASE OF ANTICIPATION AGAINST CLAIM 6

Claim 6 is separately patentable because Kida fails to disclose assigning one or more contacts of the PLD to one or more respective contacts of a second electronic component of the signal routing device based at least in part on a pattern of electrically conductive traces routed from respective contacts of the second electronic component via one or more channels formed at one or more layers of the signal routing device, as claimed. The rejection of this claim is thus improper for the reasons set forth above with respect to claim 1. In addition, Kida fails to show each and every limitation of claim 6.

6. THE EXAMINER HAS FAILED TO ESTABLISH A PRIMA FACIE CASE OF ANTICIPATION AGAINST CLAIM 7

Claim 7 is separately patentable because Kida fails to disclose assigning one or more contacts of a second PLD to one or more respective contacts of the electronic component based at least in part on a second pattern of electrically conductive traces routed from respective contacts of the electronic component via one or more channels formed at one or more layers of the signal routing device, as claimed. The rejection of this claim is thus improper for the reasons set forth above with respect to claim 1. In addition, Kida fails to show each and every limitation of claim 7.

7. THE EXAMINER HAS FAILED TO ESTABLISH A PRIMA FACIE CASE OF ANTICIPATION AGAINST CLAIM 8

Claim 8 is separately patentable because Kida fails to disclose that the one or more contacts of the PLD are assigned to the respective contacts of the electronic component by programming the PLD, as claimed. The rejection of this claim is thus improper for the reasons set forth above with respect to claim 1. In addition, Kida fails to show each and every limitation of claim 9.

8. THE EXAMINER HAS FAILED TO ESTABLISH A PRIMA FACIE CASE OF ANTICIPATION AGAINST CLAIM 9

Claim 9 is separately patentable because Kida fails to disclose that the electronic component includes one of a group consisting of: a programmable logic device (PLD) and an application specific integrated circuit (ASIC), as claimed. The rejection of this claim is thus improper for the reasons set forth above with respect to claim 1. In addition, Kida fails to show each and every limitation of claim 9.

C. THE EXAMINER HAS FAILED TO ESTABLISH A PRIMA FACIE CASE OF ANTICIPATION AGAINST CLAIM 10

Regarding claim 10, the Examiner asserts on pages 4-5 of the Office Action that Kida teaches the claimed invention. More specifically, the Examiner asserts that Kida teaches "determining a first pattern of electrically conductive traces routed from respective contacts of the electronic component via one or more channels formed at one or more layers of the signal routing device; determining a first contact assignment pattern for one or more contacts of the PLD based at least in part on the first pattern of electrically conductive traces; refining the first pattern of electrically conductive traces based at least in part on the first contact assignment pattern to generate a second pattern of electrically conductive traces

routed from the respective contacts of the electronic component via one or more channels formed at one or more layers of the signal routing device; and determining a second contact assignment pattern for one or more contacts of the PLD based at least in part on the second pattern of electrically conductive traces; wherein the one or more channels are formed by arranging vias for contacts of at least the electronic component in the signal routing device," as claimed. However, Appellants respectfully submit that the Examiner has erroneously interpreted the teachings of Kida. That is, Kida teaches:

> "providing pairs of near and far vias with the near and far vias of each pair interconnected on a surface of the apparatus by a severable trace and with all interconnection paths to or from terminal areas for use with user programmable input/output pins of the FPGA routed through at least one pair of near and far vias along at least one severable surface trace, such that selected interconnection paths of the apparatus are subject to re-working by severing selected ones of the severable traces on the surface of the apparatus and by adding jump wires over the surface of the apparatus between selected vias."

See, Column 4, lines 54-64 (emphasis added). Nowhere does Kida disclose, or even suggest, "determining a first pattern of electrically conductive traces routed from respective contacts of the electronic component via one or more channels formed at one or more layers of the signal routing device" and "refining

the first pattern of electrically conductive traces based at least in part on the first contact assignment pattern to generate a second pattern of electrically conductive traces routed from the respective contacts of the electronic component via one or more channels formed at one or more layers of the signal routing device," "wherein the one or more channels are formed by arranging vias for contacts of at least the electronic component in the signal routing device," as claimed. Indeed, Kida fails to disclose, or even suggest, in any manner, routing traces in channels and/or forming channels in one or more layers of a signal routing device by arranging vias for contacts of an electronic component in the signal routing device, as claimed. Further, Kida certainly fails to disclose, or even suggest, all of the claim elements arranged or combined in the same way as recited in the claim, as is required to establish a prima facie case of anticipation. Thus, Kida fails to disclose, or even suggest, "determining a first pattern of electrically conductive traces routed from respective contacts of the electronic component via one or more channels formed at one or more layers of the signal routing device; determining a first contact assignment pattern for one or more contacts of the PLD based at least in part on the first pattern of electrically conductive traces; refining the first pattern of electrically conductive

traces based at least in part on the first contact assignment pattern to generate a second pattern of electrically conductive traces routed from the respective contacts of the electronic component via one or more channels formed at one or more layers of the signal routing device; and determining a second contact assignment pattern for one or more contacts of the PLD based at least in part on the second pattern of electrically conductive traces; wherein the one or more channels are formed by arranging vias for contacts of at least the electronic component in the signal routing device," as claimed.

In view of the foregoing, is it respectfully submitted that claim 10 is allowable over Kida.

D. THE EXAMINER HAS FAILED TO ESTABLISH A PRIMA FACIE CASE OF ANTICIPATION AGAINST CLAIMS 11-14

Regarding claims 11-14, these claims are dependent upon independent claim 10. Thus, since independent claim 10 should be allowable as discussed above, claims 11-14 should also be allowable at least by virtue of their dependency on independent claim 10. Moreover, these claims recite additional features which are not disclosed, or even suggested, by Kida. Thus, these claims are separately patentable over Kida for at least the reasons stated below.

Appellants note that the Examiner asserts in the Office Action that claims 11-14 are rejected based upon Taylor. *See*, e.g., Office Action, page 6. The Examiner has failed to explicitly assert an obviousness rejection based upon the combination of Kida and Taylor in the Office Action. The Examiner has also failed to explicitly assert an anticipation rejection based upon Taylor alone in the Office Action. Thus, Appellants respectfully request correction of the record in this regard.

1. THE EXAMINER HAS FAILED TO ESTABLISH A PRIMA FACIE CASE OF ANTICIPATION AGAINST CLAIM 11

Claim 11 is separately patentable because Kida fails to disclose programming the PLD to assign contacts based at least in part on the second contact assignment pattern, as claimed. The rejection of this claim is thus improper for the reasons set forth above with respect to claim 10. In addition, Kida fails to show each and every limitation of claim 11.

2. THE EXAMINER HAS FAILED TO ESTABLISH A PRIMA FACIE CASE OF ANTICIPATION AGAINST CLAIM 12

Claim 12 is separately patentable because Kida fails to disclose refining the second pattern of electrically conductive traces based at least in part on the second contact assignment

pattern to generate a third pattern of electrically conductive traces routed from the respective contacts of the electronic component via one or more channels formed at one or more layers of the signal routing device, and determining a third contact assignment pattern for one or more contacts of the PLD based at least in part on the third pattern of electrically conductive traces, as claimed. The rejection of this claim is thus improper for the reasons set forth above with respect to claim 10. In addition, Kida fails to show each and every limitation of claim 12.

3. THE EXAMINER HAS FAILED TO ESTABLISH A PRIMA FACIE CASE OF ANTICIPATION AGAINST CLAIM 13

Claim 13 is separately patentable because Kida fails to disclose programming the PLD based at least in part on the third contact assignment pattern, as claimed. The rejection of this claim is thus improper for the reasons set forth above with respect to claim 10. In addition, Kida fails to show each and every limitation of claim 13.

4. THE EXAMINER HAS FAILED TO ESTABLISH A PRIMA FACIE CASE OF ANTICIPATION AGAINST CLAIM 14

Claim 14 is separately patentable because Kida fails to disclose that the electronic component includes one of a group

consisting of: a programmable logic device and an application specific integrated circuit (ASIC), as claimed. The rejection of this claim is thus improper for the reasons set forth above with respect to claim 10. In addition, Kida fails to show each and every limitation of claim 14.

E. THE EXAMINER HAS FAILED TO ESTABLISH A PRIMA FACIE CASE OF ANTICIPATION AGAINST CLAIM 15

Regarding claim 15, the Examiner asserts on pages 5-6 of the Office Action that Kida teaches the claimed invention. More specifically, the Examiner asserts that Kida teaches "an electronic component having a plurality of contacts; a programmable logic device (PLD) having a plurality of contacts; and a plurality of electrically conductive traces connecting contacts of the PLD to respective contacts of the electronic component, the plurality of electrically conductive traces routed from the respective contacts of the electronic component via one or more channels formed at one or more layers of the signal routing device; wherein the one or more contacts of the PLD are assigned based at least in part on a pattern formed by the electrically conductive traces routed from the respective contacts of the electronic component via the one or more channels, wherein the one or more channels are formed by arranging vias for contacts of at least the electronic component

in the signal routing device," as claimed. However, Appellants respectfully submit that the Examiner has erroneously interpreted the teachings of Kida. That is, Kida teaches:

> "providing pairs of near and far vias with the near and far vias of each pair interconnected on a surface of the apparatus by a severable trace and with all interconnection paths to or from terminal areas for use with user programmable input/output pins of the FPGA routed through at least one pair of near and far vias along at least one severable surface trace, such that selected interconnection paths of the apparatus are subject to re-working by severing selected ones of the severable traces on the surface of the apparatus and by adding jump wires over the surface of the apparatus between selected vias."

See, Column 4, lines 54-64 (emphasis added). Nowhere does Kida disclose, or even suggest, routing a pattern of electrically conductive traces from "respective contacts of the electronic component via one or more channels formed at one or more layers of the signal routing device; wherein the one or more contacts of the PLD are assigned based at least in part on a pattern formed by the electrically conductive traces routed from the respective contacts of the electronic component via the one or more channels, wherein the one or more channels are formed by arranging vias for contacts of at least the electronic component in the signal routing device," as claimed. Indeed, Kida fails to disclose, or even suggest, in any manner, routing traces in

channels and/or forming channels in one or more layers of a signal routing device by arranging vias for contacts of an electronic component in the signal routing device, as claimed. Further, Kida certainly fails to disclose, or even suggest, all of the claim elements arranged or combined in the same way as recited in the claim, as is required to establish a prima facie case of anticipation. Thus, Kida fails to disclose, or even suggest, "an electronic component having a plurality of contacts; a programmable logic device (PLD) having a plurality of contacts; and a plurality of electrically conductive traces connecting contacts of the PLD to respective contacts of the electronic component, the plurality of electrically conductive traces routed from the respective contacts of the electronic component via one or more channels formed at one or more layers of the signal routing device; wherein the one or more contacts of the PLD are assigned based at least in part on a pattern formed by the electrically conductive traces routed from the respective contacts of the electronic component via the one or more channels, wherein the one or more channels are formed by arranging vias for contacts of at least the electronic component in the signal routing device," as claimed.

In view of the foregoing, is it respectfully submitted that claim 15 is allowable over Kida.

F. THE EXAMINER HAS FAILED TO ESTABLISH A PRIMA FACIE CASE OF ANTICIPATION AGAINST CLAIMS 16-18

Regarding claims 16-18, these claims are dependent upon independent claim 15. Thus, since independent claim 15 should be allowable as discussed above, claims 16-18 should also be allowable at least by virtue of their dependency on independent claim 15. Moreover, these claims recite additional features which are not disclosed, or even suggested, by Kida. Thus, these claims are separately patentable over Kida for at least the reasons stated below.

Appellants note that the Examiner asserts in the Office Action that claims 16-18 are rejected based upon Taylor. *See*, e.g., Office Action, page 6. The Examiner has failed to explicitly assert an obviousness rejection based upon the combination of Kida and Taylor in the Office Action. The Examiner has also failed to explicitly assert an anticipation rejection based upon Taylor alone in the Office Action. Thus, Appellants respectfully request correction of the record in this regard.

1. THE EXAMINER HAS FAILED TO ESTABLISH A PRIMA FACIE CASE OF ANTICIPATION AGAINST CLAIM 16

Claim 16 is separately patentable because Kida fails to disclose that contacts of the PLD are assigned to the respective contacts of the electronic component by programming the PLD, as claimed. The rejection of this claim is thus improper for the reasons set forth above with respect to claim 15. In addition, Kida fails to show each and every limitation of claim 16.

2. THE EXAMINER HAS FAILED TO ESTABLISH A PRIMA FACIE CASE OF ANTICIPATION AGAINST CLAIM 17

Claim 17 is separately patentable because Kida fails to disclose that the electronic component includes one of a group consisting of: a programmable logic device and an application specific integrated circuit (ASIC), as claimed. The rejection of this claim is thus improper for the reasons set forth above with respect to claim 15. In addition, Kida fails to show each and every limitation of claim 17.

3. THE EXAMINER HAS FAILED TO ESTABLISH A PRIMA FACIE CASE OF ANTICIPATION AGAINST CLAIM 18

Claim 18 is separately patentable because Kida fails to disclose that the electrically conductive traces are routed to the respective contacts of the PLD via one or more channels formed at one or more layers of the signal routing device, as

claimed. The rejection of this claim is thus improper for the reasons set forth above with respect to claim 15. In addition, Kida fails to show each and every limitation of claim 18.

CONCLUSION

In view of the foregoing, it is respectfully submitted that the Examiner has failed to establish a prima facie case of anticipation or obviousness against the rejected claims. Thus, it is respectfully submitted that the final rejection of claims 1-18 is improper and the reversal of same is clearly in order and respectfully requested.

To the extent necessary, a petition for an extension of time under 37 C.F.R. § 1.136 is hereby made.

Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 50-0206, and please credit any excess fees to such deposit account.

Respectfully submitted,

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Date: December 22, 2008

CLAIMS APPENDIX

1 (Previously Presented). A method for mapping contacts of a programmable logic device (PLD) to contacts of an electronic component in a signal routing device having one or more layers, the method comprising:

assigning a set of one or more contacts of the PLD to one or more respective contacts of the electronic component based at least in part on a pattern of electrically conductive traces routed from respective contacts of the electronic component via one or more channels formed at one or more layers of the signal routing device, the one or more channels being formed by arranging vias for contacts of at least the electronic component in the signal routing device.

2 (Original). The method as in Claim 1, further comprising the step of forming electrically conductive traces between the set of one or more contacts of the PLD and the respective contacts of the electronic component in accordance with the pattern of electrically conductive traces.

3 (Original). The method as in Claim 2, wherein one or more of the electrically conductive traces are routed to respective contacts of the PLD via one or more channels formed at one or

more layers of the signal routing device.

4 (Original). The method as in Claim 1, further comprising the steps of:

determining a first pattern of electrically conductive traces routed from respective contacts of the electronic component via at least one channel of the one or more channels;

determining a contact assignment pattern for one or more contacts of the PLD based at least in part on the first pattern of electrically conductive traces; and

refining the first pattern of electrically conductive traces based at least in part on the first contact assignment pattern to generate a second pattern of electrically conductive traces routed from the respective contacts of the electronic component via at least one of the one or more channels.

5 (Original). The method as in Claim 4, wherein the one or more contacts of the PLD are assigned to the one or more respective contacts of the electronic component based at least in part on the second pattern of electrically conductive traces.

6 (Original). The method as in Claim 1, further comprising the step of:

assigning one or more contacts of the PLD to one or more respective contacts of a second electronic component of the signal routing device based at least in part on a pattern of electrically conductive traces routed from respective contacts of the second electronic component via one or more channels formed at one or more layers of the signal routing device.

7 (Original). The method as in Claim 1, further comprising the step of:

assigning one or more contacts of a second PLD to one or more respective contacts of the electronic component based at least in part on a second pattern of electrically conductive traces routed from respective contacts of the electronic component via one or more channels formed at one or more layers of the signal routing device.

8 (Original). The method as in Claim 1, wherein the one or more contacts of the PLD are assigned to the respective contacts of the electronic component by programming the PLD.

9 (Original). The method as in Claim 1, wherein the electronic component includes one of a group consisting of: a programmable logic device (PLD) and an application specific integrated

circuit (ASIC).

10 (Previously Presented). A method for mapping contacts of a programmable logic device (PLD) to contacts of an electronic component in a signal routing device having one or more layers, the method comprising:

determining a first pattern of electrically conductive traces routed from respective contacts of the electronic component via one or more channels formed at one or more layers of the signal routing device;

determining a first contact assignment pattern for one or more contacts of the PLD based at least in part on the first pattern of electrically conductive traces;

refining the first pattern of electrically conductive traces based at least in part on the first contact assignment pattern to generate a second pattern of electrically conductive traces routed from the respective contacts of the electronic component via one or more channels formed at one or more layers of the signal routing device; and

determining a second contact assignment pattern for one or more contacts of the PLD based at least in part on the second pattern of electrically conductive traces;

wherein the one or more channels are formed by arranging

vias for contacts of at least the electronic component in the signal routing device.

11 (Original). The method as in Claim 10, further comprising the step of programming the PLD to assign contacts based at least in part on the second contact assignment pattern.

12 (Original). The method as in Claim 10, further comprising the steps of:

refining the second pattern of electrically conductive traces based at least in part on the second contact assignment pattern to generate a third pattern of electrically conductive traces routed from the respective contacts of the electronic component via one or more channels formed at one or more layers of the signal routing device; and

determining a third contact assignment pattern for one or more contacts of the PLD based at least in part on the third pattern of electrically conductive traces.

13 (Original). The method as in Claim 10, further comprising the step of programming the PLD based at least in part on the third contact assignment pattern.

14 (Original). The method as in Claim 10, wherein the electronic component includes one of a group consisting of: a programmable logic device and an application specific integrated circuit (ASIC).

15 (Previously Presented). A signal routing device having one or more layers and further comprising:

an electronic component having a plurality of contacts;

a programmable logic device (PLD) having a plurality of contacts; and

a plurality of electrically conductive traces connecting contacts of the PLD to respective contacts of the electronic component, the plurality of electrically conductive traces routed from the respective contacts of the electronic component via one or more channels formed at one or more layers of the signal routing device;

wherein the one or more contacts of the PLD are assigned based at least in part on a pattern formed by the electrically conductive traces routed from the respective contacts of the electronic component via the one or more channels, wherein the one or more channels are formed by arranging vias for contacts of at least the electronic component in the signal routing device.

16 (Original). The signal routing device as in Claim 15, wherein contacts of the PLD are assigned to the respective contacts of the electronic component by programming the PLD.

17 (Original). The signal routing device as in Claim 15, wherein the electronic component includes one of a group consisting of: a programmable logic device and an application specific integrated circuit (ASIC).

18 (Original). The signal routing device as in Claim 15, wherein the electrically conductive traces are routed to the respective contacts of the PLD via one or more channels formed at one or more layers of the signal routing device.

EVIDENCE APPENDIX

[NONE]

RELATED PLEADINGS APPENDIX

[NONE]